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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,278	01/22/2002	Shawn Peter Bawell	17797	6773

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EXAMINER
TAKAOKA, DEAN O

ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 04/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/055,278	BAWELL ET AL.	
	Examiner	Art Unit	
	Dean O Takaoka	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,17,19-21,23 and 24* is/are rejected.

7)☒ Claim(s) *16,18 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities: Fig. 1 is shown as "Prior Art" but is not disclosed as such in the "Brief Description of the Drawings", with respect to Fig. 1 (page 6, line 21; e.g. Fig. 2).

Appropriate correction is required.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "terminating elements are Field Effect Transistors" (claim 20) and "paddle" (claim 22) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

With respect to claim 20, it appears the only terminating elements shown are pin diodes and not FET's (e.g. Fig. 5).

With respect to claim 22, no "paddle" appears to be shown (e.g. page 15, lines 1 – 4). While discussed with respect to the prior art, it does not appear to be shown with respect to the current invention.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The applicant is required to provide a copy of the drawings with proposed drawing changes marked in red ink as required by 37 CFR 1.121(d).

Claim Objections

Claim 15 objected to because of the following informalities: The Examiner believes wording "is comprises" is a typographical error and suggests to delete the word [is].

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 12, 15, 17, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Halloran (U.S. Patent No. 5,463,355).

Claim 12:

Halloran (Figs. 2 and 3) shows a circuit (e.g. modulator elements) for performing vector modulation (abstract, spec all), the circuit encapsulated within a chip scale package, comprising: an MMIC (col. 4, line 10); a plurality of terminating elements (loads 14b, c, d connected to each modulator).

Claim 15:

Where the MMIC comprises a layer of GaAs (col. 2, lines 8,9).

Claim 17:

Where the MMIC is configured to comprise: an input quadrature hybrid; a first quadrature hybrid and a second quadrature hybrid; and an output power combiner (where Halloran shows an input power divider 16, a modulator 12a – e, and an output

power combiner 17; where elements 16, 12 and 17 are all quadrature hybrids as is well-known, further illustrated by Swarup (US Patent No. 5,929,729) – col. 4, lines 11-16, where three-port couplers are commonly known a power divider/combiners and four ports couplers are commonly known as quadrature couplers).

Claim 21:

Where the number of terminating elements used equal four (four resistor terminating elements 14 b-e).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 – 4 and 7 – 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Drapac (U.S. Patent No. 3,988,705) in view of Caragliano et al. (U.S. Patent No. 3,999,150).

Claim 1:

Drapac (Fig. 1) show a circuit functioning as a quadrature hybrid (couplers 10, 12, 14, 38).

Drapac shows the quadrature hybrid using generic couplers but does not show a specific coupler such a well-known art-recognized equivalent spiral coupler.

Caragliano (Figs. 6, 6a and 9) shows a well-known art-recognized equivalent spiral coupler having a plurality of inductors (adjacent spiral windings shown in 6a and

9) and a plurality of capacitances (where Kozak discloses parasitic capacitances – col.10, line 9) where all capacitances are intrinsic (e.g. parasitic capacitances).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the well-known generic couplers disclosed by Drapac with the well-known art-recognized equivalent spiral coupler disclosed by Caragliano. Such a modification would have been a mere substitution replacing the generic coupler with the well-known art-recognized equivalent spiral coupler thus suggesting the obviousness of the modification.

Claim 2:

Caragliano shows the plurality of spiral inductors comprising an insulating layer disposed between the first and second spiral inductors (best illustrated by dimension X in Fig. 6a or 2XB +ΔB in Fig. 9), where the first and second spiral layer are positioned relative to each other to create an intrinsic capacitance (where intrinsic capacitances Cs and Cm are discussed, e.g. col. 4 with respect to the prior art of Figs. 1 and 2 which correlate to Fig. 3b which correlates to the spacing X shown in Figs. 6a and Fig. 9, thus the first and second spiral layer are obviously positioned relative to each other to create an intrinsic capacitance) .

Claim 3:

Where the first and second spiral inductor are aligned (shown in Fig. 6a of Caragliano et al.).

Claim 4:

A first output and a second output, where the second output is approximately ninety degrees different in phase in comparison to the first output (shown by Drapac in Fig. 1 where the phase difference is 90°).

Claim 7:

Drapac and Caragliano et al. teach the quadrature hybrid circuit including couplers comprising spiral inductors in the reasons for rejection of claim 2 above.

Caragliano et al. shows an example where the area for the spiral length of the first and second spiral inductors is 3.2" x 3.2" with a spaced distance of 0.24" for a frequency of 8MHz (col. 8, lines 5-8) but does not teach the overall length and width dimension of 200um x 200um.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the area disclosed by Drapac and Caragliano et al. with the area of 200um x 200um disclosed by the claim. Such a modification would have been obvious in that the dimensional area, e.g. electrical length of the inductors is dependent upon factors such as the desired frequency, pitch of the lines, and dielectric constant selected. Since the desired frequency is not provided, such as in the example given by Caragliano et al. (8MHz – col. 8, line 3), it would have been obvious to have modified the coupler of Drapac and Caragliano et al. with an area of 200um x 200um to meet a desired frequency in a given application where the length and width of the spiral inductor lines are 200um x 200um thus suggesting the obviousness of the modification.

Claims 8 – 10:

Drapac and Caragliano et al. teach the quadrature hybrid circuit including couplers comprising spaced spiral inductors comprising intrinsic capacitance in the reasons for rejection of claim 2 above.

Caragliano et al. teaches where the area for the spiral length of the first and second spiral inductors is 3.2" x 3.2" with a spaced distance of 0.24" for a frequency of 8MHz (col. 8, lines 5-8) but does not teach the equation for intrinsic capacitance of the claim.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have determined the spacing between coupled inductors capacitance disclosed by Drapac and Caragliano et al. with the formula for capacitance disclosed by the claim. Such a use of the well-known capacitance formula would have obvious in that the formula of the claim is a standard well-known formula for capacitance derived from any fundamental electronics book (e.g. formula 9.10 – Boylestad), further where Caragliano et al. teaches the distance of the spaced spiral inductor lines, dielectric strength of the insulator, area of the spiral lines and pitch of lines for an exemplary frequency of 8MHz thus suggesting the obviousness of the formula.

Claim 11:

A third output terminated to ground (18 – Fig. 1) via a 50 ohm termination (where Drapac teaches a 50 ohm termination – col. 1, lines 5 – 8).

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Drapac and Caragliano et al. as applied to claim 2 above, and further in view of Pan (U.S. Patent No. 4,511,813).

Claim 5:

Drapac and Caragliano et al. teach the quadrature hybrid circuit including couplers comprising spiral inductors in the reasons for rejection of claim 2 above.

Drapac and Caragliano et al. are silent where the first and second spiral inductors and the insulating layer are contained on a MMIC.

Pan (Fig. 12) shows a similar quadrature hybrid circuit where the couplers are contained on a MMIC (col. 1, line 45 to col. 2, line 7; col. 2, line 63 to col. 3, line 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the quadrature hybrid circuit including couplers comprising spiral inductors disclosed by Drapac and Caragliano et al. with the similar quadrature hybrid circuit where the couplers are contained on a MMIC disclosed by Pan. Such a modification would have realized the advantageous benefit of providing a MMIC quadrature hybrid circuit with low cost, miniaturization, and high reliability (Pan – col. 1, lines 46-48) thus suggesting the obviousness of the modification.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Drapac and Caragliano et al. as applied to claim 2 above, and further in view of Itoh (U.S. Patent No. 4,914,407).

Claim 6:

Drapac and Caragliano et al. teach the quadrature hybrid circuit comprising a coupler with an insulating layer in the reasons for rejection of claim 2 above.

Caragliano et al. teaches a generic insulating layer but is silent where the insulating layer comprises Silicon Nitride.

Itoh (Fig. 2) shows a device such as a coupler (col. 1, lines 16-17) where an insulative layer comprises Silicon Nitride (30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the quadrature hybrid circuit including couplers comprising spiral inductors disclosed by Drapac and Caragliano et al. with the similar quadra-ture hybrid circuit where the couplers are contained on a MMIC disclosed by Pan. Such a modification would have realized the advantageous benefit of providing a MMIC quadrature hybrid circuit with low cost, miniaturization, and high reliability (Pan – col. 1, lines 46-48) thus suggesting the obviousness of the modification.

Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halloran in view of Caragliano et al. (U.S. Patent No. 3,999,150).

Claim 13:

Halloran teaches the circuit comprising a plurality of well-known generic quadrature hybrids (e.g. modulators comprising 90° couplers) each comprising a plurality of inductors (obvious in that each coupler comprises a plurality of inductors, e.g. at least two and a plurality of capacitances, also obvious in that any two coupled transmission lines would inherently have parasitic, e.g. intrinsic capacitances).

Halloran does not show where the well-known generic couplers each comprise a first and second spiral inductor; an insulating layer between the spiral inductors where the insulating layer is positioned relative to each other to create an intrinsic capacitance.

Caragliano et al. (Figs. 6 – 9) shows a well-known art-recognized equivalent spiral coupler comprising a plurality of inductors comprise a well-known first spiral inductor and a second spiral inductor; the circuit further comprising an insulating layer disposed between the first and second spiral inductors (best illustrated by dimension X in Fig. 6a or 2XB +ΔB in Fig. 9), where the first and second spiral layer are positioned relative to each other to create an intrinsic capacitance (where intrinsic capacitances Cs and Cm are discussed, e.g. col. 4 with respect to the prior art of Figs. 1 and 2 which correlate to Fig. 3b which correlates to the spacing X shown in Figs. 6a and Fig. 9, thus the first and second spiral layer are obviously positioned relative to each other to create an intrinsic capacitance) .

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the well-known generic coupler disclosed by Halloran with the well-known art-recognized equivalent spiral coupler disclosed by Caragliano et al. Such a modification would have been a mere substitution of well-known art-recognized equivalent couplers thus suggesting the obviousness of the modification.

Claim 14:

Halloran and Caragliano et al. teach the quadrature hybrid circuit including couplers comprising spiral inductors in the reasons for rejection of claim 12 above.

Caragliano et al. shows an example where the area for the spiral length of the first and second spiral inductors is 3.2" x 3.2" with a spaced distance of 0.24" for a frequency of 8MHz (col. 8, lines 5-8) but does not teach the size of the chip scale package is approximately 4mm x 6mm.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the area disclosed by Halloran and Caragliano et al. with the area of 4mm x 6mm disclosed by the claim. Such a modification would have been obvious in that the dimensional area, e.g. electrical length of the inductors is dependent upon factors such as the desired frequency, pitch of the lines, and dielectric constant selected. Since the desired frequency is not provided, such as in the example given by Caragliano et al. (8MHz – col. 8, line 3), it would have been obvious to have modified the coupler of Halloran and Caragliano et al. with an area of 4mm x 6mm to meet a desired frequency in a given application where the length and width of the spiral inductor lines are 4mm x 6mm thus suggesting the obviousness of the modification.

Claims 19, 20, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halloran and Caragliano et al. as applied to claim 12 above, and further in view of Pan (U.S. Patent No. 4,511,813).

Claims 19 and 20:

Halloran teaches the quadrature hybrid circuit in the reasons for rejection of claim 12 above.

Halloran shows hybrid coupler circuit including resistive terminations (14b – d) but does not show the terminations being diodes or FET's.

Pan (Fig. 12) shows a similar hybrid coupler circuit including terminations (101-104) comprising diodes or FET's (col. 10, lines 13-28).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the terminations disclosed by Halloran with the terminations being diodes or FET's disclosed by Pan. Such a modification would have realized the advantageous benefit of providing weighting elements to provide gain control of an amplifier (as illustrated in Figs. 16 and 18 with respect to the circuit of Fig. 12 shown by Pan) thus suggesting the obviousness of the modification.

Claim 23:

Pan shows bias control to FET (Fig. 13) thus it would also be obvious to include bias control to the diodes since Pan teaches that diodes where conventionally used or where the FET of Pan's invention would replace the diode.

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Halloran.

Claim 24:

Halloran shows the circuit for performing vector modulation, discussed in the reasons for rejection of claim 12 above.

Halloran shows a generic MMIC circuit with circuit connections but does not explicitly show the physical package.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the generic circuit disclosed by Halloran with the actual I/O pins disclosed by the claim. Such a modification would have obvious in that Halloran shows the input (Lo) and output (output link) thus it would have been obvious to include actual I/O pins in a circuit to facilitate the connection thus suggesting the obviousness of the modification.

Allowable Subject Matter

Claim 16, 18, and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dean O Takaoka whose telephone number is (703) 305-6242. The examiner can normally be reached on 8:30a - 5:00p Mon - Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (703) 308-4909. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

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April 15, 2003

Robert Pascal
Supervisory Patent Examiner
Technology Center 280